HL1361BRxx-Lx

DFB Laser Diode Chip Bar

Sample Categories and Disclaimer

Functional sample that has the suffix of "-F" or "-Fx" to the product number is a sample that is designed according to the customer's request. The purpose of this sample is to check and confirm the product feasibility. Thus the sample may be an R&D prototype or may be a modified current product. This sample may not be manufactured in qualified production lines nor using qualified parts. Basically Oclaro guarantees the requested performance of BOL (Beginning Of Life). Any qualification will not be applied.

Working sample that has the suffix of "-W" or "-Wx" to the product number is a sample to evaluate, confirm and finalize the product specifications. Basically Oclaro guarantees the performance of BOL (Beginning Of Life). Not all qualifications may be completed. This sample may not be manufactured in qualified production lines nor be using qualified components. Until Oclaro Inc. releases the products for general sales, Oclaro Inc. reserves the right to change prices, features, functions, specifications, capabilities and release schedule.

DESCRIPTION

General

The HL1361BRxx-Lx is a Distributed Feed-Back (DFB) laser diode chip bar. The lasing wavelength is in the 20nm spacing CWDM range. Individual chip is designed for 10Gbit/s operation. One bar contains 34pcs or 35pcs of LD chips in line.

PN information

The PN is common to both Type A and Type B.

PN	PN (initial samples)	Chip qty in a bar	Wavelength* Lx (nm)
HL1361BRxx-L0	HL1361BRxx-L0-F	34 or 35	1270
HL1361BRxx-L1	HL1361BRxx-L1-F	34 or 35	1290
HL1361BRxx-L2	HL1361BRxx-L2-F	34 or 35	1310
HL1361BRxx-L3	HL1361BRxx-L3-F	34 or 35	1330

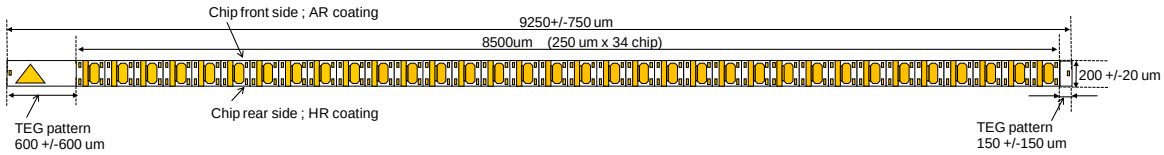
* Actual wavelength range is specified separately.

Outline

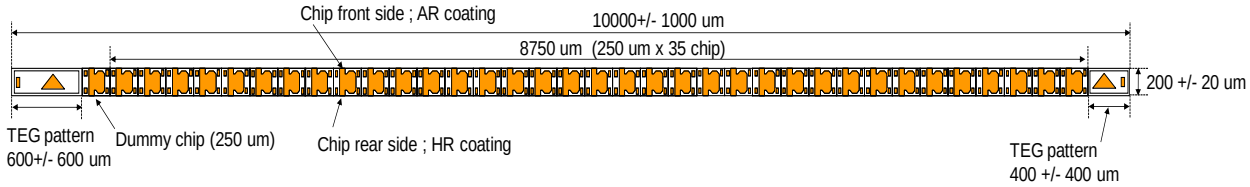
Bar Dimension

The bar will have either Type A or Type B.

Type A



Type B



Pin Configurations

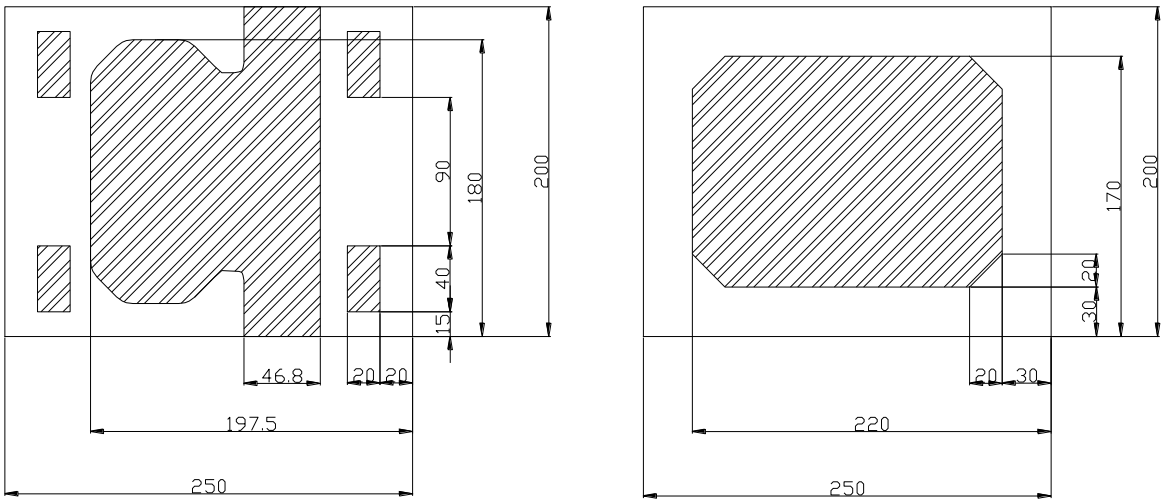
Fig 1. Block Diagram (one LD chip)

Table 1. Pin Configurations

Pin #	Description	Remarks
1	Laser anode (P electrode)	
2	Laser cathode (N electrode)	

MECHANICAL DIMENSIONS

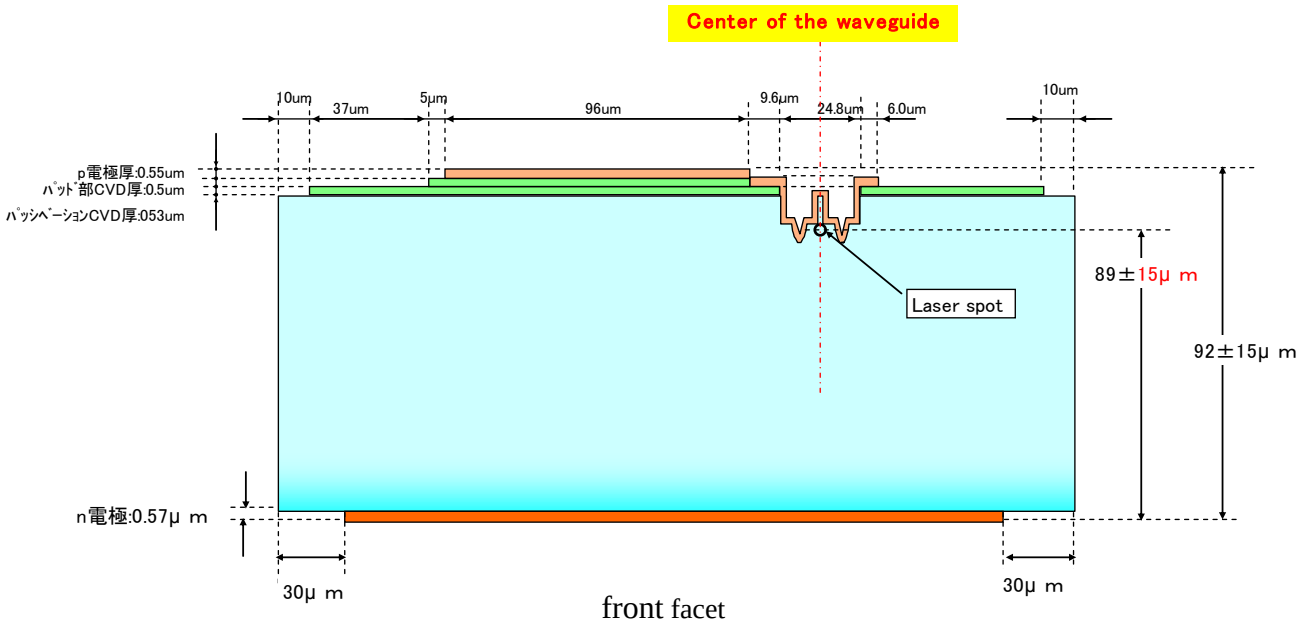
Individual chip size is 250 μm x 200 μm x 92 μm. Fig. 3 shows a chip outline and metallization pattern. The Anode has typ. 0.55um Au film and Cathode has typ. 0.57um Au film respectively.



Light output direction

Top view (Anode)

Bottom view (Cathode)



front facet

(Outline:+/-20um)

Fig 3 Chip Outline and Dimensions

PERFORMANCE SPECIFICATIONS

Absolute Maximum Ratings

Since the HL1361BRxx-Lx-x is a bar form, the performance will depend on not only chip performance but also its assembling process including dicing. If the chip is assembled in a proper way, the performance described in Table 2 can be expected but these are not guaranteed values. Oclaro assumes no responsibility for those reliability when they are assembled and/or tested in customer Tc means submount temperature when the chip mounted on Oclaro standard sub-mount soldered on heat sink.

Table 2. Absolute Maximum Ratings (Tc=25°C, unless otherwise specified)

	Absolute Maximum Rating	Min	Max	Unit	
1	Storage temperature	-40	85	C	
2	Operating temperature	-40	95	C	Hermetically sealed
3	Laser forward bias current	-	150	mA	
4	Laser reverse bias voltage	-	2	V	
5	Die binding temperature	-	350	C	(< 4 s) Note

Note: Recommended condition: 320 C max and 4 s max.

Optical and Electrical Characteristics

Since the HL1361BRxx-Lx-x is a bar form, the performance will depend on not only chip performance but also its assembling process including dicing. If the chip is assembled in a proper way, the performance described in Table 3 can be expected but these are not guaranteed values.

Table 3. Expected Optical and Electrical Characteristics
(Tc= -5C to 95C, unless otherwise specified, Condition at CoC(Chip on testing carrier))

No	Optical and Electrical Characteristics	Min	Typ	Max	Units	Notes
1	Wavelength range	-7.3	Lx	+9.7	nm	at operating output power
2	Wavelength at 25C	-4	Lx	+2	nm	Ditto At 25 C
3	Wavelength temperature coefficient	-	0.1	0.11	nm/degC	For reference only
4	Trise/Tfall (20-80%)	-	30	-	ps	For reference only
5	Side-mode suppression ratio (SMSR), operating condition	35	-	-	dB	
6	Threshold current @ 25C	-	8	15	mA	
7	Threshold current @ 95C	-	20	28	mA	
8	Slope efficiency @ 25C, I=Ith+5mA to I=Ith+50mA	-	0.3	-	W/A	
9	Slope efficiency @ 95C, I=Ith to I=70mA	0.11	-	-	W/A	
12	Mask Margin (IEEE 10.3Gb/s) I=Ith+25mA @25C	20	-	-	**%**	PRBS=2^{31}-1, 1k waveforms TOSA ER=4.5dB
13	Front/back output power ratio, 33mA(1C), 70mA(95C)	1	4	10	-	
14	Effective serial resistance, per lane	4	7	10	Ohms	
15	Laser forward voltage	-	1.3	2	V	
16	Kink deviation, Ith+5 to Ith+75mA	-	-	20	%	See figure 2
17	Far field divergence angle, vertical @85C, I=Ith+30mA	-	35	45	degrees	40 deg max by 99% distribution
18	Far field divergence angle, horizontal@ 85C, I=Ith+30mA	-	32	40	degrees	36 deg max by 99% distribution

Note: Tc means sub-mount temperature when the chip mounted on Oclaro standard sub-mount soldered on a heat sink.

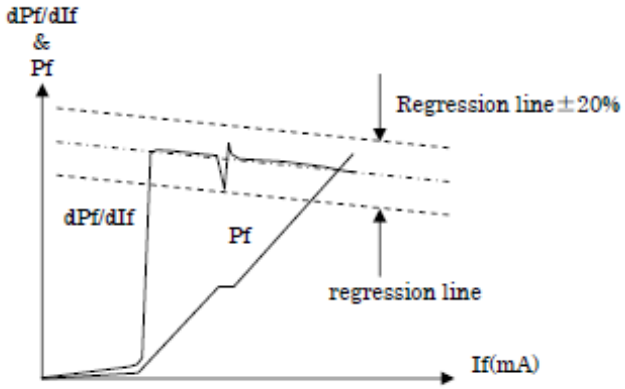


Fig 2 Kink definition

VERIFICATION PROCESS

Oclaro will carry out the following verification test.

The bar samples will be picked up from the specified area of the finished wafer, i.e. center and middle circumferences.

- Pulse testing: shown in Table 4

- Burn-in testing: shown in Table 5 using the chips on carrier which passed the Pulse testing

- DC testing and checking the criteria: shown in Table 5

Table 4 Chip pulse test criteria (Ts=25°C, unless otherwise specified)

No.	Parameter	Symbol	Condition	Min	Max	Unit	Remark
1	Threshold current	I_{th}	T_s=85°C	—	22	mA	
2	Slope efficiency	Eta	T_s=85°C, I_F=67.5mA	0.13	—	W/A	Using OPM standard tester
3	Peak wavelength	λ_p	I_F=67.5mA	—	—	nm	NA
4	Side mode suppression ratio	SMSR	I_F=67.5mA	35	—	dB	
			I_F=67.5mA	35	—	dB	

Ts means stage temperature in pulse chip test.

Table 5 Criteria in wafer verification test

Parameter	Condition	Pass Criterion	Minimum Number or Yield
LD chip mount	-	-	20pcs
Start Burn-In test			
Optical Purge test	25°C, 120mA, ACC 3min.	$\|\Delta I_{th}\| \leq +5\%$, $\|\Delta Po\| \leq +10\%$, $\|\Delta Eta\| \leq +10\%$.	
Electrical Purge test	100°C, 150mA, ACC 20h	-	
APC Test	95°C, 70mA, AAPC 100h, $(I_{op}@100h-I_{op}@0h)/I_{op}@0h$	$-2\% \leq \Delta I_{op} \leq$ **+0.5%**	
Pass Burn-In test			
Start DC test			
Threshold current	T_c=95°C	$I_{th} \leq 28mA$	
Slope efficiency	T_c=95°C, Eta≡Po(70mA)/(70mA-I_{th})	Eta≥0.11W/A	
Forward voltage	T_c=1°C, I_o=33mA T_c=95°C, I_o=70mA	$V_{op} \leq 1.8V$	
Optical output power	T_c=1°C and 95℃, 70mA	kink free	
Peak wavelength L0	T_c=1°C, I_o=33mA	1265.2nm≤λp≤1277.5nm	
	T_c=95°C, I_o=70mA		
Peak wavelength L1	T_c=1°C, I_o=33mA	1285.2nm≤λp≤1297.5nm	
	T_c=95°C, I_o=70mA		
Peak wavelength L2	T_c=1°C, I_o=33mA	1305.2nm≤λp≤1317.5nm	
	T_c=95°C, I_o=70mA		
Peak wavelength L3	T_c=1°C, I_o=33mA	1325.2nm≤λp≤1337.5nm	
	T_c=95°C, I_o=70mA		
Side mode suppression ratio	T_c=1℃, Io=33mA T_c=95°C, I_o=70mA	SMSR≥35dB	
Beam divergence angle (Horizontal)	T_c=95°C, I_o=70mA	FWHM_H≤36deg	
Beam divergence angle (Vertical)	T_c=95°C, I_o=70mA	FWHM_V≤40deg	
Pass DC test			10 of 20pcs (50%)

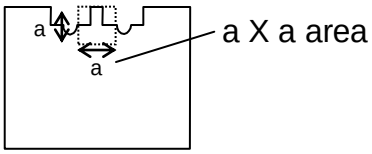
VISUAL INSPECTION CRITERIA

Visual inspection of the bar

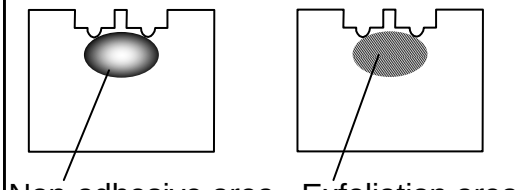
Oclaro will carry out 100% bar visual testing by x200 microscope but not for individual chips. The criteria are shown in Table 6. It is assumed that more than 90% chips in the bar have no defectives in the ***a × a area*** defined as below. Oclaro assumes no responsibility for bar failed at the customer (buyer) for quantity up to 4% of shipping lot.

Table 6

Definition of a X a area



Front/rear facet of the chip

	Defectives Items	Defectives
1	Exfoliation of films	 Non-adhesive area and/or Exfoliated area inside a X a area.

Chip pulse testing

Oclaro will not carry out individual chip pulse testing for shipping.

OTHER SPECIFICATIONS

Packing and label

The products will be packed as described in Fig. 4 below.

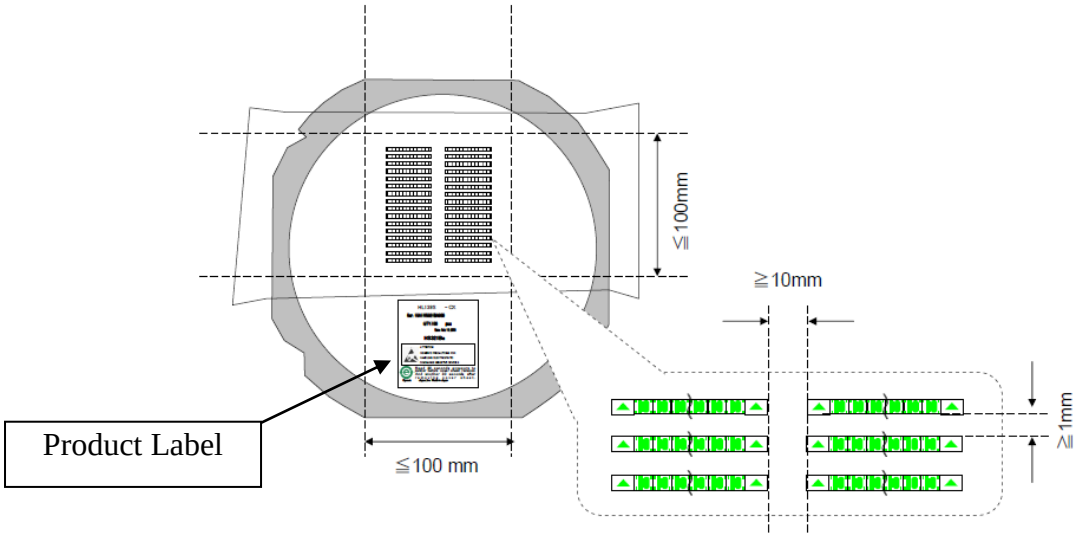


Fig 4 Packing format

(LD bars shown above are not the actual reduced scale)

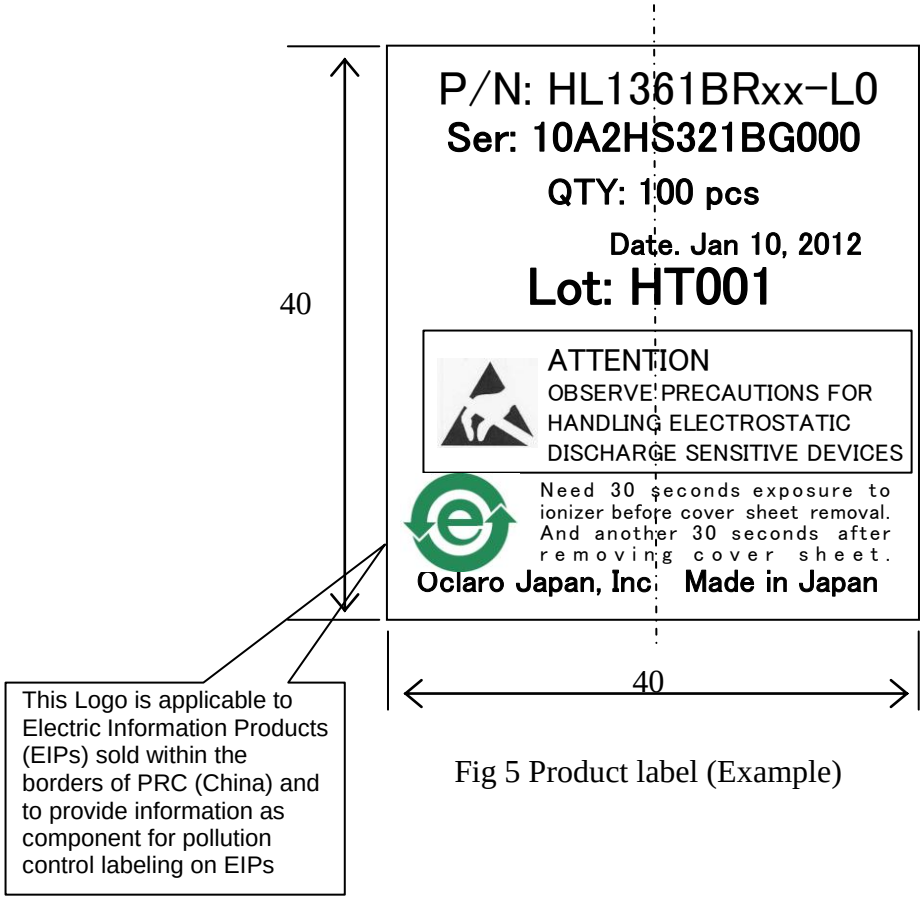


Fig 5 Product label (Example)

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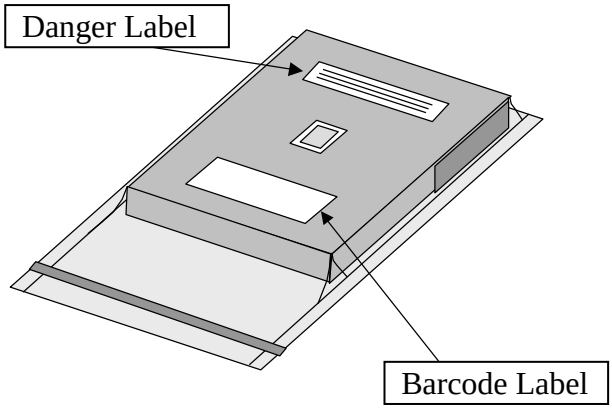

The plastic bag is vacuum-packed.

Fig 6 Packing bag (Example)

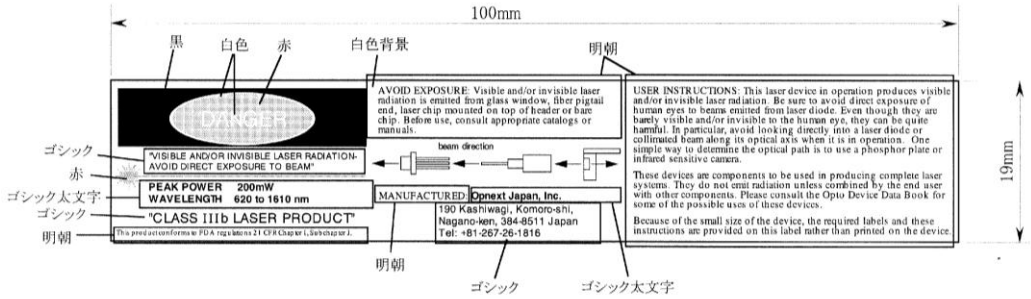

Fig 7 Danger Label (Example)

Bar code label is on plastic bag for each shipment form. Supplier Product Name, Supplier lot number, the Quantity and Part Number are on it. Please see Fig.8. 40x 80 mm

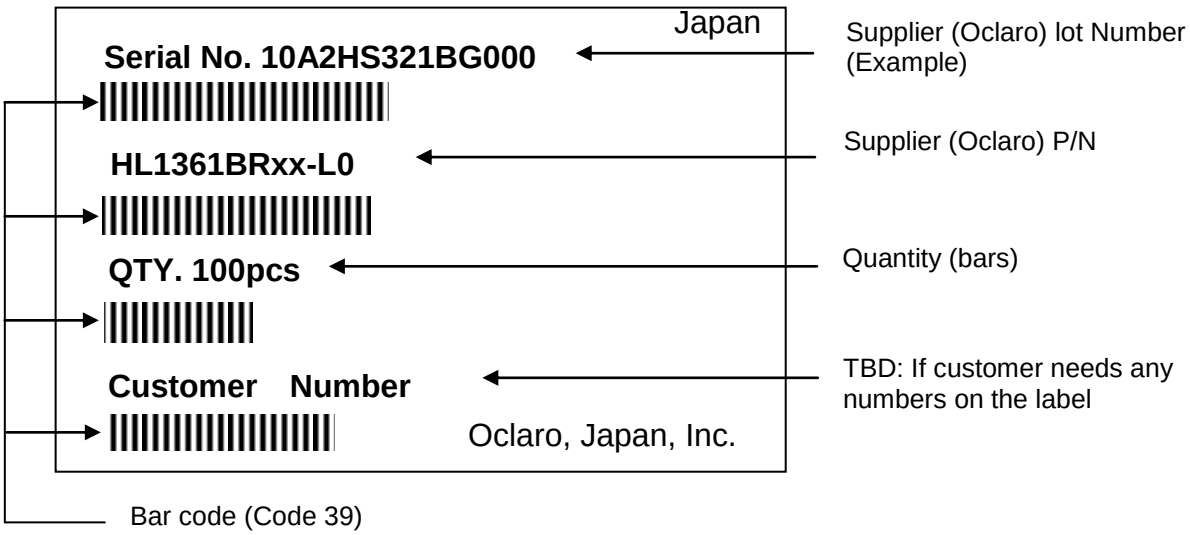

Fig. 8 Bar code label on outer plastic bag (Example of HL1361BRxx-L0)

USER INFORMATION

Handling Precautions

(1) Dicing

Since the HL1361BRxx-Lx-x is a bar form, the dicing process requires proper handling.

1. Not to put any excess stress to the active layer of the laser chip in vending the bar for dicing. Applying the appropriate scribing to the separation portion for guiding is recommended.
2. In case of using laser scriber, prevent from adverse affect to the active layer of the laser chip by way of optimize the laser power, time and any conditions of the laser scriber.

(2) Electrostatic Discharge

This device may be damaged by electrostatic discharge. Take proper electrostatic-discharge (ESD) precautions while handling these devices.

Revision History

Rev.	Date	Page/Line/Fig/Table	Modification	Note
0.0	Jul 16, 2014			
1.0	Dec 02, 2015	P1 P2 P4/Table2	Added new PN Delete 22pcs bar and added 35pcs bar Changed operating temp -5 min➔-40 min	